What Is Claimed Is:

1. A data transfer control device, connected with a primary PCI bus, secondary PCI bus and external storage device, for controlling access of said primary PCI bus and said secondary PCI bus with said external storage device, comprising:

a P-PCI bus side counter circuit for counting the transfer period of said primary PCI bus by clock cycle count;

an S-PCI bus side counter circuit for counting the transfer period of said secondary PCI bus by clock cycle count;

a scheduler circuit for controlling assert timing of TRDY# of said primary PCI bus and access of said primary PCI bus and said secondary PCI bus by the counter value of said P-PCI bus side counter circuit and counter value of said S-PCI bus side counter circuit;

an arbiter circuit for arbitrating access of said primary PCI bus and said secondary PCI bus according to the control of said scheduler circuit;

an S-PCI bus interface circuit to be an interface for accessing of said secondary PCI bus to said external storage device according to the arbitration of said arbiter circuit;

a P-PCI bus interface circuit for interfacing access between said primary PCI bus and said external storage device according to the arbitration of said arbiter circuit and arbitrating the assert timing of TRDY# according to the control of said scheduler; and

a memory interface circuit for arbitrating access of said primary PCI bus or said secondary PCI bus to said external storage device, wherein

when access of said secondary PCI bus to said external storage device is generated while said primary PCI bus is executing burst transfer to said external storage device, assert of a TRDY# signal of the burst transfer of said primary

PCI bus to said external storage device just before access of said secondary PCI bus to said external storage device is delayed such that the period until assert of a TRDY# signal of next burst transfer of said primary PCI bus to said external storage device would satisfy a standard value for burst transfer continuation.

2. A data transfer control device, connected with a primary PCI bus, secondary PCI bus and external storage device, for controlling access of said primary PCI bus and said secondary PCI bus with said external storage device, comprising:

a P-PCI bus side counter circuit for counting the transfer period of said primary PCI bus by clock cycle count;

an S-PCI bus side counter circuit for counting the transfer period of said secondary PCI bus by clock cycle count;

a scheduler circuit for controlling assert timing of TRDY# of said primary PCI bus and access of said primary PCI bus and said secondary PCI bus by the counter value of said P-PCI bus side counter circuit and the counter value of said S-PCI bus side counter circuit;

an arbiter circuit for arbitrating access of said primary PCI bus and said secondary PCI bus according to the control of said scheduler circuit;

an S-PCI bus interface circuit to be an interface for accessing of said secondary PCI bus to said external storage device according to the arbitration of said arbiter circuit;

a P-PCI bus interface circuit for interfacing access of said primary PCI bus to said external storage device according to the arbitration of said arbiter circuit and arbitrating the assert timing of TRDY# according to the control of said scheduler; and

a memory interface circuit for arbitrating access of said primary PCI bus or said secondary PCI bus to said external storage device, wherein

when a plurality of accesses of said secondary PCI bus to said external storage device is generated while said primary PCI bus is executing burst transfer to said external storage device, access of said primary PCI bus to said external storage device and access of said secondary PCI bus to said external storage device are repeated, and assert of a TRDY# signal of the burst transfer of said primary PCI bus to said external storage device just before each access of said secondary PCI bus to said external storage device is delayed such that the period until assert of a TRDY# signal of next burst transfer of said primary PCI bus to said external storage device would satisfy a standard value for burst transfer continuation.

3. A data transfer control device, connected with a primary PCI bus, secondary PCI bus and external storage device, for controlling access of said primary PCI bus and said secondary PCI bus with said external storage device, comprising:

a scheduler circuit for controlling access of said primary PCI bus and said secondary PCI bus, disconnecting said primary PCI bus and requesting access of said secondary PCI bus to said external storage device when access of said secondary PCI bus to said external storage device is generated while said primary PCI bus is executing burst transfer to said external storage device, and then successively requesting access of said primary PCI bus to said external storage device;

an arbiter circuit for arbitrating access of said primary PCI bus and said secondary PCI bus according to the control of said scheduler circuit;

an S-PCI bus interface circuit to be an interface for accessing of said secondary PCI bus to said external storage device according to the arbitration of said arbiter circuit;

a P-PCI bus interface circuit for interfacing access of said primary PCI bus to said external storage device according to the arbitration of said arbiter circuit; and

a memory interface circuit for arbitrating access of said primary PCI bus or said secondary PCI bus to said external storage device, wherein

when access of said secondary PCI bus to said external storage device is generated while said primary PCI bus is executing burst transfer to said external storage device, transfer of said primary PCI bus to said external storage device is prepared while said secondary PCI bus is accessing said external storage device.

4. The data transfer control device according to any one of Claims 1 to 3, wherein said external storage device has a 32-bit data bus width, and both the burst transfer of said primary PCI bus to said external storage device and access of said secondary PCI bus to said external storage device are executed in 32-bit units.

5. The data transfer control device according to any one of Claims 1 to 3, wherein said external storage device has a 16-bit data bus width, and a 32-bit burst transfer of said primary PCI bus to said external storage device is executed dividing into upper and lower 16-bits each, and access of said secondary PCI bus to said external storage device is also executed in 16-bit units.